UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

A-S

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/247,974	02/11/99	YING T	TS98-518

IM62/0110

STEPHEN B ACKERMAN
20 MCINTOSH DRIVE
POUGHKEEPSIE NY 12603

EXAMINER	
TRAN, B	
ART UNIT	**PAPER NUMBER**
1765	7

DATE MAILED: 01/10/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/247,974	Ying et al.
Examiner	**Group Art Unit**
Binh Tran	1765

☒ Responsive to communication(s) filed on *Feb 11, 1999*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-26* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-26* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 6

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3, 6, 9, 11, 14-15, 18, 22, 24, 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 3, 18, " wiring structure to be applied" is vague and indefinite. It is unclear whether any wiring structure is applied or not.

In claims 6, "said etch back to be performed" is vague and indefinite. It is unclear whether any etch back is performed or not.

In claims 9, 22, "said layer to be deposited" is vague and indefinite.

In claims 11, 15, 24, 26, "high dielectric constant" is vague and indefinite.

3. Claim 14 recites the limitation "spacers" in claim 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 8, 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicholls et al. (US 5,602,055) in view of Lee (US 5,663,092).

Nicholls discloses a method comprising the steps of:

depositing a first layer of dielectric (Fig 2 Ref 28) over said wiring structure (Fig 2 Ref 26) thereby including the exposed surface of the semiconductor substrate;

depositing a second layer of dielectric material over the first layer of dielectric;

etching the second dielectric layer to remove in its totality except where the second dielectric layer forms spacers on the sidewalls of the wiring structure;

depositing a dielectric layer over spacers on the sidewalls of the wiring structure, over first dielectric layer on the bottom of the holes within the wiring structure, and over first dielectric overlaying the top surfaces of the wiring structure.

Nicholls further discloses the wiring structure contains an electrically conducting material such as polysilicon; the second dielectric layer covers the surface of the first dielectric layer on the bottom of the holes and further covers the first dielectric layer on top surface of the wiring structure (col 3).

Nicholls does not disclose the step of etching back the first layer of dielectric, or the wiring structure contains a lower layer of polysilicon and an upper layer of silicon nitride, or the second dielectric layer further covers the surface of the partially exposed top corners of the wiring

structure, or the dielectric material is deposited over the spacers and also over the exposed top corner of the wiring structure, or the step of planarizing the deposited PE-oxide layer down to the plane of the top surface.

In a self aligned contact, Lee discloses the step of etching back the dielectric layer form on top of the wiring structure; the wiring structure contains a lower layer of polysilicon and an upper layer of silicon nitride; the second dielectric layer is silicon nitride and it covers the partially exposed of the wiring structure. Lee further discloses the use of silicon oxide or TEOS as the dielectric material that is deposited over the spacers (col 5) and also over the exposed top corner of the wiring structure (Fig 8, Ref 120, 123, 125 and 128); the step of planarizing (using CMP) the oxide layer down to the plane of the top surface (col. 5 line 38-41).

Lee does not disclose the use of plasma enhance for silicon oxide or plasma enhance TEOS, however Lee does disclose the use of TEOS for dielectric layer. Further the use of Plasma enhanced for TEOS is well known in the semiconductor art (See prior art made of record).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nicholls in view of Lee by etching back the dielectric layer form on the top of the wiring structure because etching back will remove extra portions of dielectric layer that form during the deposition process.

It would have been obvious one having ordinary skill in the art at the time the invention was made to modify Nicholls in view of Lee by depositing a second dielectric layer so that it

covers the partially exposed of the wiring structure; and depositing layer of oxide over the spacers and partially over the exposed top corner of the wiring structure because these dielectric layers will protect the wiring structure during etching steps.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nicholls in view of Lee by depositing a layer of PE-oxide or PE-TEOS over the spacers because Nicholls is not particular about the kind of dielectric material and therefore any dielectric material would have been anticipated to produce an expected result.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nicholls in view of Lee by utilizing silicon nitride as the second dielectric layer because silicon nitride is cheap to make. Further, Nicholls is not particular about the kind of material for his dielectric layer and therefore any dielectric material would have been anticipated to produce an expected result.

Regarding to claim 3, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nicholls in view of Lee by utilizing the wiring structure contains a lower polysilicon and an upper layer of silicon nitride because the silicon nitride will act as the mask to protect the lower polysilicon layer.

Regarding to claim 5, Nicholls and Lee are silent whether the dielectric layer contains high density plasma oxide. However the use of high density plasma oxide is well known in semiconductor art (See Yao et al. (US 5,814,654)). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nicholls and Lee by utilizing

high density plasma oxide for the dielectric layer because Nicholls and Lee are not particular about the kind of dielectric oxide material and therefore any dielectric oxide would have been anticipated to produce an expected result.

6. Claims 6-7, 16-21, 24, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicholls and Lee , and further in view of Jeng et al. (US 5,683,922).

Both Nicholls and Lee are silent about the use of Buffered Oxide Etch (BOE) for etching back the first dielectric layer.

In a self-aligned contact, Jeng discloses the wet etching using 20:1 BOE etchant for dielectric layer (abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nicholls and Lee in view of Jeng by utilizing buffered oxide etch for etching back the dielectric layer because BOE etchant increases the selectivity of the silicon oxide/silicon nitride layer.

Claims 7, 21 further differ from Jeng by the specific value of an etchant ratio in the BOE solution. It would have been prima facie obvious to employ any of a variety of etchant ratio in the BOE solution including those claimed by the applicant, this is well-known variable in the wet etching art which is known to effect both the rate and quality of the wet etching process. Further, the selection of particular values for this variable would simply involve routine experimentation and would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nicholls and Jeng in view of Lee by including additional step of planarizing the deposited layer of PE-oxide or PE-TEOS down to the plane of the top surface because planarizing will remove the rough surface during deposition steps.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nicholls and Lee as applied to claim 1 above, and further in view of Liaw (US 5,807,779). Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nicholls, Lee and Jeng as applied to claim 16 above, and further in view of Liaw (US 5,807,779).

Nicholls and Lee are silent about using PECVD to deposit a layer of silicon nitride to a thickness about 1000 -2000 Angstroms at the temperature of 400 °C.

In a self-aligned contact, Liaw teaches to deposit silicon nitride using PECVD to a thickness about 1000 Angstroms (col 4 line 15-18). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nicholls and Lee in view of Liaw by utilizing PECVD at 400 °C to deposit silicon nitride because PECVD is easy and effective procedure for depositing silicon nitride. Further, it would be obvious to modify Liaw by using different temperature because routine experimentation would have been expected to optimize the temperature.

8. Claims 10,13, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicholls and Lee as applied to claim 1 above, and further in view of Kasai (US 5,821,594). Claims

23, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicholls, Lee and Jeng as applied to claim 16 above, and further in view of Kasai (US 5,821,594).

Claims 10, 23 differ from Nicholls, Lee and Jeng by specifying aluminum oxide (Al_2O_3) as the material for the second dielectric layer. Claims 13, 25 differ from Nicholls, Lee and Jeng by further specifying CHF_3 as the etchant gas for silicon nitride at flow rate of 15 sccm, pressure of about 15 mtorr, rf power density of about 700 watts with no magnetic field and ambient wafer temperature of 15°C.

In a self-aligned contact, Kasai discloses the dielectric layer may be selected from the group consisted of silicon nitride, silicon nitric oxide and alumina (a.k.a. aluminum oxide) (col. 3 line 40-45). Kasai further discloses the use of CHF_3 as the etchant gas for a silicon nitride layer.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nicholls and Lee in view of Kasai by utilizing aluminum oxide as the material for the second dielectric layer because equivalent and substitution of one for the other would have been anticipated to produce an expected result.

Claims 13, 25 further differ from Kasai by the specific value of etchant gas flow rate, gas pressure, rf power density. It would have been prima facie obvious to employ any of a variety of etchant gas flow rates, gas pressures, rf power densities including those claimed by the applicant. These are all well known variables in the plasma etching art which is known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for this

variable would simply involve routine experimentation and would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hsu et al. (US 5,663,578) disclose a thin film transistor with self-aligned bottom gate and depositing the silicon oxide by PE-TEOS. Bronner et al. (US 5,792,703), Para et al. (US 5,731,242) and Lin (US 5,668,065) disclose a self-aligned contact for the wiring process. Tsai et al. (US 5,851,890) disclose a notched sidewall spacer.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh X. Tran whose telephone number is (703) 308-1867.

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

Binh X. Tran

January 6, 2000